SPECIFICATION

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[*METHOD AND RELATED CIRCUIT FOR CLOCK GENERATION AND RECOVERY*]

Background of Invention

[0001] 1.Field of the Invention

[0002] The present invention relates to a method and related circuit for clock generation and recovery, and more particularly, to clock generation and recovery in an optical disk drive.

[0003] 2.Description of the Prior Art

[0004] In this modern information based society, one of the major concerns is how to manage and store tremendous amounts of information. Compared to other kinds of storage media, the compact disk has a small size and a higher-density storage capacity. Due to developments in recordable and rewritable compact disk technology, consumers have the ability to utilize compact disk storage capacity on their personal computers.

[0005] In order to effectively manage the information stored on a compact disk, the data storage region of the compact disk is divided into many frames. Data can be stored in these frames according to a memory format. Each frame is identified by a minute/second, which means that a given frame corresponds to a particular time. The related time signal is known as the absolute time in pre-groove (ATIP).

[0006]

A top view of a typical compact disk 10 is shown in Fig. 1. As is well known in the art, the compact disk 10 comprises a reflecting surface 13. A compact disk drive emits a laser beam onto the reflecting surface 13 of the compact disk 10, and the laser

beam is reflected by different parts of the reflecting surface 13. The compact disk drive reads the information on the compact disk by collecting the reflected laser beam using an optical pickup.

[0007] On the reflecting surface 13 of the compact disk 10, there is a fine spiral track 11. Please refer to Fig. 1, which shows a magnified view 1A of the fine track 11. The track 11 is composed of two types of tracks, one being a data track 12 to record data, and the other being a wobble track 14 to record related time information of each frame. As illustrated in the magnified view 1A, the data track 12 has a continuously spiral shape, and the wobble track 14 has an oscillating shape. Additionally, the curvature of the wobble track 14 is composed of small segment curves with two different periods, D1 and D2.

[0008] In a further magnified view 1B in Fig. 1, an interrupt and discontinuity record mark 16 is shown within data track 12. The length of each record mark 16 varies, and the reflection characteristic of the record mark 16 is different from that of the reflecting surface 13. The record mark 16 is used to allow the compact disk drive to be able to write data onto the compact disk 10. The surface of the wobble track 14 protrudes beyond the reflecting surface 13. The data track 12 is located inside a groove formed by the raised wobble track 14 as is shown in Fig. 2, which is a three-dimensional perspective view of the magnified view 1B of the compact disk 10.

[0009] The process used to control the optical pick up in the compact disk drive to extract data from the wobble track 14 will now be explained using Fig.3. As the compact disk rotates, an optical pick up 20 can be thought of as moving over the track 11 of the compact disk along the direction of arrow 18. In addition to a optical receiver (not shown) for reading the data from record mark 16 within the data track 12, there are four sensors within the optical pick up 20, namely Sa, Sb, Sc, and Sd. These four sensors are utilized to extract information from the wobble track 14. The positions of sensors Sa and Sd are controlled to be located within the groove of wobble track 14.The positions of sensors Sb and Sc are controlled to be located in the protruded area of the wobble track 14. The reflected laser beam intensities detected by the four sensors Sa, Sb, Sc, and Sd are different because of the difference in reflecting quality between the groove and the protruded area of the wobble track 14.

As the optical pick up 20 moves along a straight path from the position shown to position P1, the sensing values of the four sensors Sa, Sb, Sc, and Sd change. A wobble signal can be generated by subtracting the electrical sensing value of Sa from that of Sd.

[0010] A waveform diagram of the wobble signal is shown in Fig. 4 with time along the abscissa and waveform amplitude along the ordinate. As described previously, the sensing values of the sensors Sa, Sb, Sc, and Sd change with time because the pick-up head 20 will detect different locations of the wobble track 14 when the compact disk 10 keeps rotating. This causes the wobble signal to change in amplitude with time. The curvature of the wobble track 14 is composed of two different curves with two different periods, D1 and D2. Consequently, the wobble signal waveform is also composed of two different curves with two different periods, T1 and T2, corresponding to the two periods, D1 and D2. Time information related to the control of the compact disk drive is stored by the changing period of the wobble track 14 and present in the wobble signal.

[0011] Waveform diagrams of the information associated with the wobble signal are shown in Fig. 5, which has time along the abscissa. Fig.5 shows a wobble signal 22, an ATIP signal 24, a data clock signal 26, and a time data signal 28. After undergoing a waveform clipping process, the sinusoidal wobble signal in Fig. 4 is transformed into the square wave wobble signal 22. The integrity of the different periods, T1 and T2, is maintained in the new wobble signal 22. The portion of the wobble signal 22 with the period T1, and frequency 1/T1, corresponds to a high level signal in the ATIP signal 24. Likewise, portion of the wobble signal with the period T2, and frequency of 1/T2, corresponds to a low level signal in the ATIP signal 24. As a result, the time data corresponding to the record related area of the compact disk can be extracted from the wobble signal 22 using frequency demodulation.

[0012]

The extraction of time data 28 is done using both the ATIP signal 24 and the data clock signal 26. As shown in Fig. 5, the data clock signal 26 is utilized to synchronize the reading of the ATIP signal 24.The ATIP signal 24 is read at each clock pulse in the clock signal 26 to generate the sequential bit sequence shown in the time data signal 28. A period TB of the data clock signal 26defines the time duration of one bit in the

ATIP signal 24. Through analysis of the time data 28, the information stored in the related records of the compact disk can be found and extracted. Also, when writing data to the compact disk, the data to be stored on the compact disk can be put into the correct record area.

[0013] The compact disk drive alsoutilizes a wobble clock to assist in the generation of the wobble signal. The wobble clock frequency is related to the average frequency of the changing frequencies, 1/T1 and 1/T2, in the wobble signal. The average frequency is close to (1/T1 + 1/T2)/2 with little deviation, and the frequency of wobble clock is normally twice as high as this average frequency.

[0014] A functional block diagram of a prior art data circuit 30 is shown in Fig. 6. The block diagram explains how a time data signal 50 and a wobble clock 48 are obtained from a wobble signal 32. Fundamentally, the prior art circuit 30 is very similar to a phase-locked loop (PLL). After the wobble signal 32 is determined, the wobble signal 32 is operated on by a pre-processing circuit 34, which is usually a frequency divider, and then fed to an input 36A of a phase comparator 36. The phase comparator 36 compares two input signals from two inputs, 36A and 36B, and outputs a corresponding signal to an output 36C according to the comparison result. The output 36C of the phase comparator 36 is connected to a low pass filter 40. The low pass filter 40 smoothes the signal from the phase comparator 36 and generates a control signal at node 38. As shown in Fig. 6, the control signal output at node 38 is provided to a wobble clock generator 46, a voltage controlled oscillator (VCO) 42, and a waveform shaping circuit 52. The wobble signal 32 contains two different frequencies, 1/T1 and 1/T2, and the control signal at node 38 reflects this. Specifically, the control signal changes with the changing frequency of the wobble signal 32, and forms a control waveform signal. The control waveform signal at node 38 is further processed by the waveform shaping circuit 52 and output as a time data signal 50. Similarly, the control waveform signal at node 38 is processed by the wobble clock generator 46 to create the wobble clock 48. In order for the circuit 30 to function like a PLL, the control voltage at node 38 is fed to a voltage controlled oscillator to generate a period signal. The period signal is further handled by a feedback processing circuit 44, which is functionally related to the pre-processing circuit 34, and then fed-back to the input 36B of the phase comparator 36 as a

reference level for comparison. The reference level is utilized by the phase comparator 36 to distinguish between the different frequencies of the wobble signal 32.

[0015] The prior art circuit 30 has the major disadvantage of being designed using analog components. The charge pump in the phase comparator 36, the capacitors and resistors of the low pass filter 40 and the voltage controlled oscillator 42, are all analog components. Conversely, the data processing and signal controlling circuit modules in the compact disk drive are realized by programmable digital integrated circuits, such as digital signal processing chips. Combining analog and digital circuits is expensive and labor intensive.

Summary of Invention

[0016] It is therefore a primary objective of the claimed invention to provide a method and related circuit using cost-effective and laborsaving digital circuit design to solve the above-mentioned problem of the prior art analog circuit.

[0017] According to the claimed invention, the data circuit comprises a reference clock generator to generate a reference clock, a counter, a digital average processor to calculate an average number, a frequency divider to generate a wobble clock, a comparator to generate an absolute time in pre-groove(ATIP) signal, a waveform shaping processor to shape the ATIP signal into a time data signal, and a synchronizer to generate an ATIP clock.

[0018] According to the claimed invention, the method for recovering an ATIP clock and an ATIP signal from the wobble signal comprises counting the number of reference periods of a reference clock contained within a period of the wobble signal, and generating a corresponding counting result. The method further comprises, generating an average number according to the long-term average of the counting result, generating a wobble clock according to the average number and the counting result, and generating the ATIP clock according to the ATIP signal and the wobble clock.

[0019] It is an advantage of the claimed invention that the data circuit uses only digital components.

[0020] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0021] Fig.1 is a top view of a compact disk according to the prior art.

[0022] Fig.2 is a perspective diagram of a portion of a reflecting surface of the compact disk shown in Fig.1.

[0023] Fig.3 is a schematic diagram showing a wobble tracking process of the compact disk shown in Fig.1.

[0024] Fig.4 is a waveform diagram of a wobble signal according to the prior art.

[0025] Fig.5 is a diagram of waveforms of the wobble signal from Fig.4, an ATIP signal, a data clock signal, and a time data signal according to the prior art.

[0026] Fig.6 is a functional block diagram of a prior art data circuit.

[0027] Fig.7 is a functional block diagram of a data circuit according to the present invention.

[0028] Fig.8 is a diagram of waveforms of a wobble signal, and a counting result.

[0029] Fig.9 is a diagram of waveforms of an ATIP signal, a wobble clock, and a time data signal.

[0030] Fig.10 is a functional block diagram of the synchronizer shown in Fig.7.

[0031] Fig.11 is a state diagram of the status generator shown in Fig.10.

[0032] Fig.12 is a diagram of waveforms of a wobble clock, an ATIP clock, and related signals.

Detailed Description

[0033]

The functional block diagram of a data circuit 60, in accordancewith a preferred embodiment of the claimed invention, is shown in Fig. 7. The data circuit 60

comprises a reference clock generator 62 to generate a reference clock 66, a counter 72, a digital average processor 74 to calculate an average number 76, a frequency divider 68 to generate a wobble clock 70, a comparator 78 to generate anabsolute time in pre-groove (ATIP) signal 80, a waveform shaping processor 82 to shape the ATIP signal 80 into a time data signal 84, and a synchronizer 86 to generate anATIP clock 88.

[0034] After extracting a wobble signal 64 from a compact disk, the wobble clock 70, the time data signal 84, and the corresponding ATIP clock 88 are generated by signal analysis of the wobble signal 64 by the data circuit 60. The sensors of an optical pick up in a compact disk drive are able to reada wobble track on a compact disk.The wobble signal 64, which is the same as a wobble signal 22 shown in Fig. 5, can be obtained from signal analysis of the sensing values. The main function of the data circuit 60 is to generate the wobble clock 70, a time data signal 84, and theATIP clock 88 based on the wobble signal 64.

[0035] The function of the data circuit 60 according to the present invention will now be described in detail. The reference clock generator 62 generates the reference clock 66 with a fixed frequency. The reference clock 66 can be either aneight-to-fourteen modulation clock in the compact disk drive or a system clock in the data circuit 60. The frequency of the reference clock 66 is much higher than two different frequencies, 1/T1 and 1/T2, in the wobble signal 64. Since the frequency of the reference clock 66 is fixed, a reference period of the reference clock 66 is also fixed. Both the reference clock 66 and the wobble signal 64 are input to the counter 72, and the counter 72 counts the number of periods of the reference clock 66 occurring within a period of the wobble signal 64 to generate a corresponding counting result 73. Please refer to Fig. 8, which provides a clear picture of the counting process for the wobble signal 64. Both the waveforms of the wobble signal 64 and the counting result 73 at a node 72A are shown in Fig. 8.

[0036]

Referring to Fig.8, the wobble signal 64 is composed of different segments with two different frequencies. Consequently, the wobble signal 64 comprises durations TP2 and TP4, which have a period T1, and the durations TP1 and TP3, which have a period T2. Taking advantage of the reference period T3 as a measuring unit, the

counter 72 evaluates the number of reference periods T3 occurring within a single period of the wobble signal 64. A period T2 of the wobble signal 64 is shown magnified as 8A. In the same way, a period T1 of the wobble signal 64 is shown magnified as 8B. Since the frequency of the reference clock 66 is much higher than the frequencies 1/T1 and 1/T2, the reference period T3 is much smaller than the periods T1 and T2. Typically, the reference period T3 is about one hundred times shorter than the period T1 or T2. The counter 72 counts the number of reference periods T3 during a single period T1 or T2 and outputs the counting result 73 to the node 72A, in Fig.7. Because the period T2 is shorter than the period T1, the number of reference periods 73 occurring in the period T2 is smaller than the number of reference periods 73 occurring in the period T1. The duration TP1 or TP3 of the wobble signal 64 with frequency 1/T2 is determined to have a low counting result 73. Conversely, the duration TP2 or TP4 of the wobble signal 64 with frequency 1/T1 is determined to have a high counting result 73. As is shown in Fig. 8, a waveform of the counting result 73 changes in signal level according to the different frequencies of different segments of the wobble signal 64.

[0037] The counting result 73 of counter 72 is provided to the digital average processor 74 to determine a long-term average number 76, which is also shown in Fig. 8. The frequency of wobble clock 70 corresponds to the average frequency of the wobble signal 64, and the frequency of wobble clock 70 is usually twice the average frequency of wobble signal 64. The average number 76 is a long-term average of the counting result 73 generated from the wobble signal 64. That is, the average number 76 is related to the wobble signal 64. Accordingly, the wobble clock 70 can be generated by a suitable frequency dividing process on the reference clock 66 by the frequency divider 68. Specifically, a wobble clock 70, with a frequency twice as high as the average frequency of the wobble signal 64, can be generated by controlling the dividing ratio of the frequency divider 68 to be a half of the average number 76. In other words, a wobble clock 70 is obtained by simply dividing the reference clock 66 by half of the average number 76. The wobble clock 70 is output by the data circuit 60 and used to control the rotating speed of compact disk in the compact disk drive.

[0038] The counting result 73 is also utilized to generate the time data signal 84. As mentioned, the waveform of the counting result 73 is similar to the waveform of the

time data signal 84 and a simple method to transform the counting result 73 into the time data signal 84 will now be described. Both the average number 76 and the counting result 73 are input to the comparator 78. The comparator 78 outputs a high signal level when the counting result 73 is larger than the average number 76 and a low signal level when the counting result 73 is smaller than the average number 76. The comparison result between counting result 73 and average number 76 generated by comparator 78 is output to form the ATIP signal 80. Since the ATIP signal 80 may not be synchronized with wobble clock 70 and the waveform may not be shaped adequately, the ATIP signal 80 is fed to the waveform shaping processor 82. The waveform shaping processor 82 is able to generate a time data signal 84, which is synchronized with the wobble clock 70, with the aid of a triggering process.

[0039] The synchronizing process for the time data signal 84 is illustrated in Fig. 9, which shows waveforms of the ATIP signal 80, the wobble clock 70, and the time data signal 84.In Fig.9, time is along the abscissa. The waveform shaping processor 82 samples the ATIP signal 80 at the falling edge 70A of the wobble clock waveform 70. For instance, the waveform shaping processor 82 samples a low level signal ofthe ATIP signal 80 at a time ta, and holds the low level signal for the time data signal 84 for the duration of the period of wobble clock 70. Likewise, the waveform shaping processor 82 samples a high level signal of the ATIP signal 80 at a time tb, and holds the high level signal for time data signal 84 for the duration of the period of wobble clock 70. Consequently, the rising edge of time data signal 84 is aligned with the falling edge of the wobble clock signal 70, and the time data signal 84 is thus synchronized with the wobble clock 70. In this way, the waveform shaping processor 82 synchronizes the ATIP signal 80 to form the time data signal 84.

[0040] After the time data signal 84 is formed, both the time data signal 84 and the wobble clock 70 are fed into the synchronizer 86 to generate the corresponding ATIP clock 88. The signal processing of the synchronizer 86 is illustrated in a functional block diagram Fig.10. As shown in Fig.10, the synchronizer 86 comprises a status generator 90 used to generate a status signal 92, and a period counter 94 used to generate the ATIP clock 88. Based on the signal level of time data signal 84 and the triggering of the wobble clock 70, the status generator 90 generates a status signal 92. Under the reset control of status signal 92 and the triggering of the wobble clock

70, the period counter 94 can accumulate a number of periods to generate the ATIP clock 88.

[0041] For further explanation of the operation of synchronizer 86, please refer to Fig.11, which is a state diagram of the status generator 90. In Fig.11, state 1 represents a high level and state 0 represents a low level of the time data signal 84. When triggered by the rising edge of wobble clock signal 70, the status generator 90 detects the signal level of the time data signal 84. If the signal level of the time data signal 84 is low, corresponding to state 0, the status signal 92 generated by the status generator 90 becomes or remains in state 0. If the signal level of time data signal 84 then becomes high, the status signal 92 will switch to state 1. Additionally, if the signal level of time data signal 84 remains constant, the status signal 92 will be held in the corresponding state. Finally, if the signal level of time data signal 84 changes from high to low, the status signal 92 will switch from state 1 to state 0. The status generator 90 outputs the status signal 92 in this manner.

[0042] Please refer to Fig. 12, having a time scale along the abscissa, for waveform diagrams of the time data signal 84, the wobble clock 70, the status signal 92, a number of periods96 of the period counter 94, and the ATIP clock 88. As mentioned previously, the status generator 90 determines the signal level of status signal 92 using the time data signal 84 according to the triggering signal of the rising edge of the wobble clock 70. For instance, before a time tc, the signal level of the time data signal 84 is low, and the status signal 92 is accordingly maintained at state 0. However, at the time tc, the status generator 90 switches the status signal 92 from state 0 to state 1. After the time tc and until a time td, and since time data signal 84 remains at a high level, the status signal 92 is held in state 1. The period counter 94 resets the counted number of periods 96 when the status signal 92 changes. For instance, the period counter 94 resets the number of periods 96 at the times tc and td. The period counter 94 generates the ATIP clock 88 according to some rule using the number of periods 96 counted. For example, if a period TB of the ATIP clock 88 consists of six periods of the wobble clock 70, then the period counter 94 generates pulses of the ATIP clock 88 at the times when the value of number of periods 96 is 3, 9 (3+6), 15 (3+2*6), etc. TheATIP clock 88 is thus generated by the above extraction process performed on the data signal 84.

[0043] The present invention has been described referencinga preferred embodiment. The feature in which six periods of wobble clock 70 represent one pulse of theATIP clock 88 is described in detail only for better understanding of the operation of the present invention. Generally, if the period ofthe ATIP clock 88 is to consist of N periods of the wobble clock 70, the period counter 94 will generate the pulses of the ATIP clock 88 at the times when the value of number of periods 96 is N/2, N/2+N, and N/2+2N etc.In the general case, the difference between two consecutive values of the counted number of periods 96 for generating the ATIP clock 88 is N. The number N is determined when the wobble clock 70 is generated by frequency divider 68.

[0044] Base on the above explanation of the present invention, the data circuit 60 of the present invention essentially comprises a counter and a logic processing circuit, which are designed using well known digital circuits and clock triggering processes, to generate the wobble clock 70, the time data signal 84, and the corresponding ATIP clock 88. Utilizing these signals, the compact disk drive is able to control the rotation speed of the compact disk, and thus able to extract all the record related information on the compact disk. In addition, the teachings of the present invention can be easily applied to different control modes of the compact disk drive, such as constant angular velocity (CAV) mode, and constant linear velocity (CLV) mode.

[0045] Compared to the prior art, which uses an analog phase-locked loop, the present invention is realized with a modern digital logic design. The present invention can therefore be easily integrated into the digital control modules of compact disk drives. All of the related manufacturing processes, from circuit design and simulation to production, can be based on the development processes of digital circuit modules. Thus, the labor saved in development and the costs reduced in production are the major advantages of the present invention.

[0046] Those skilled in the will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.